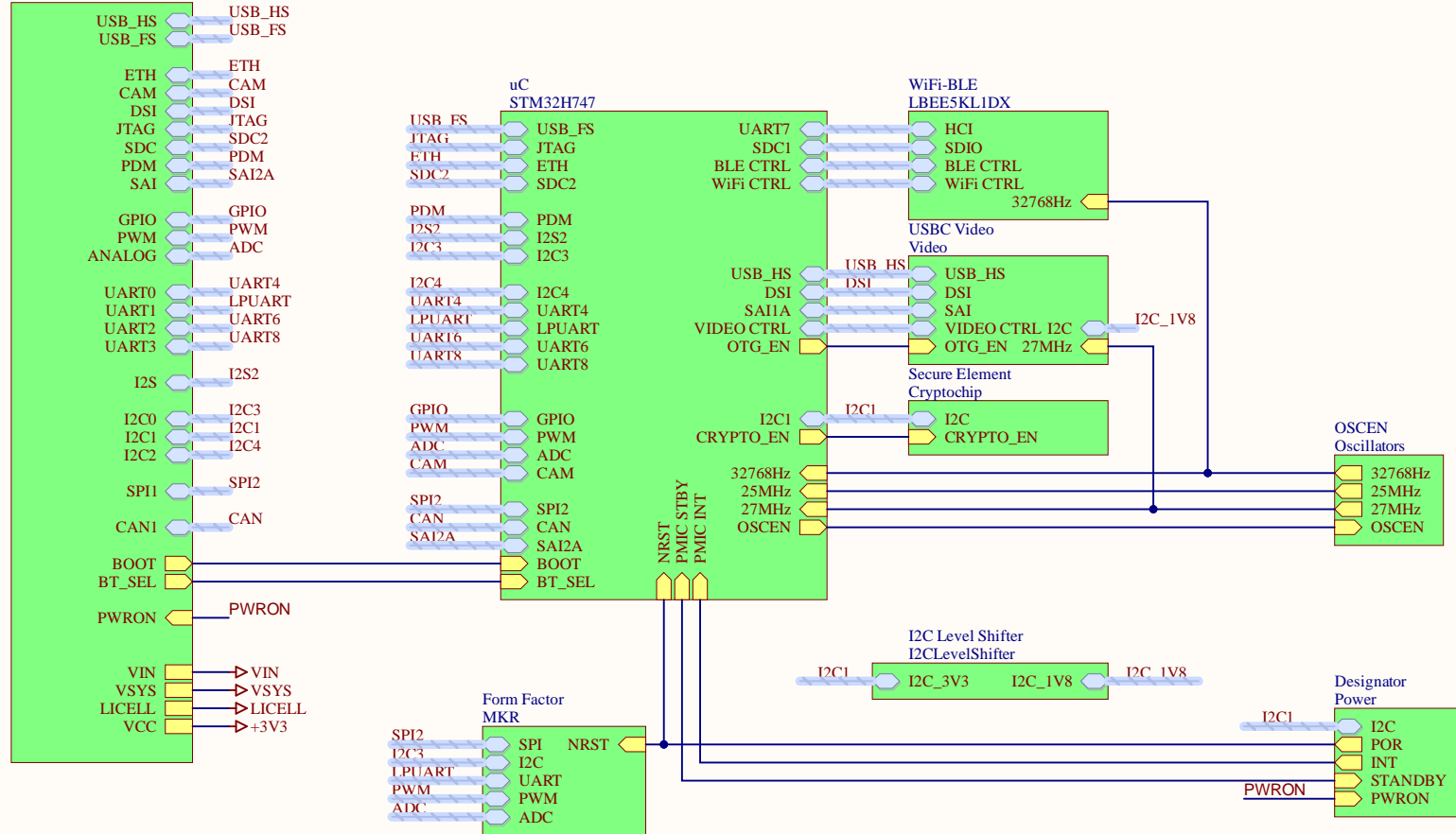
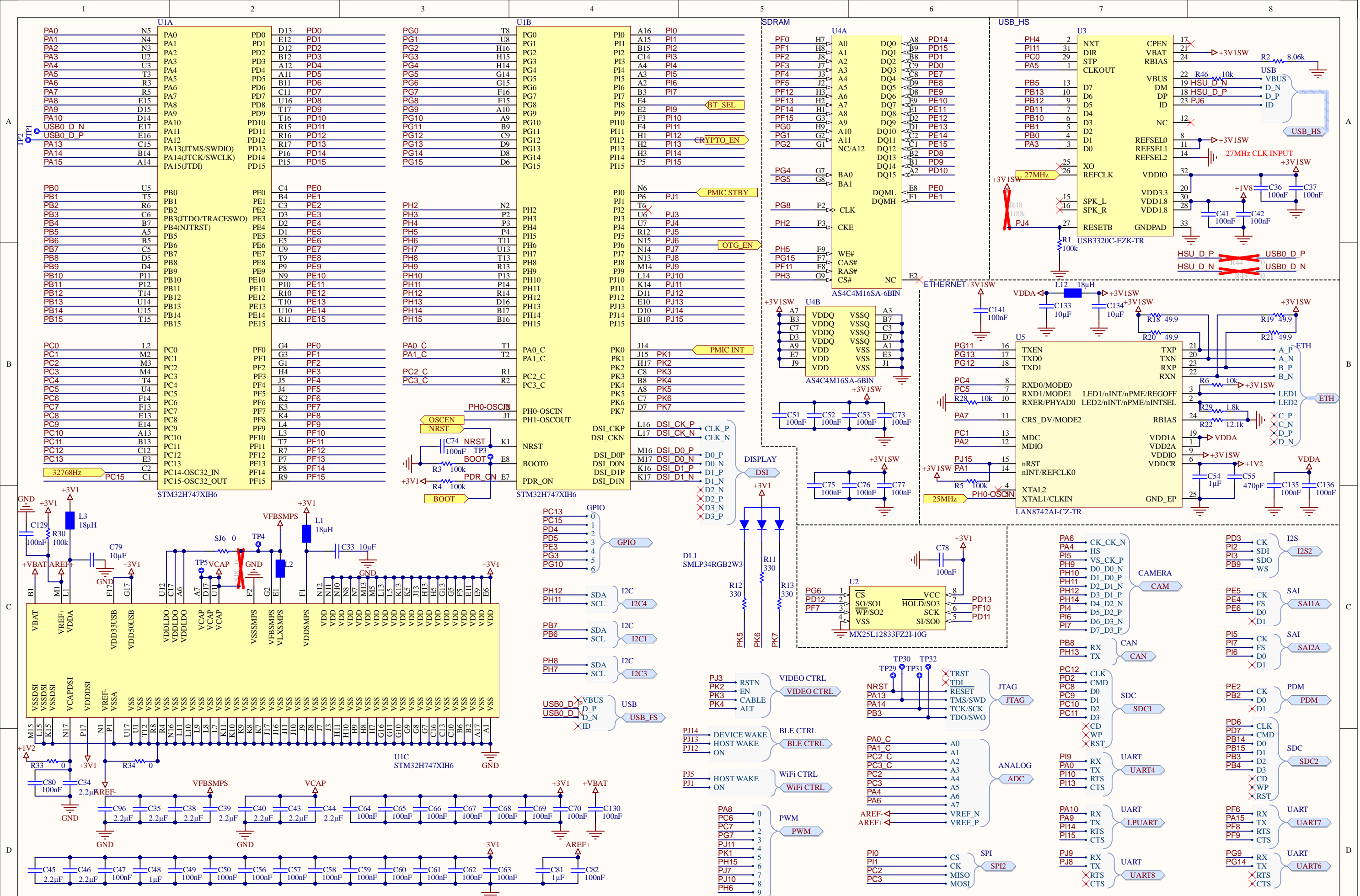


HDCConnectors
HDCConn.SchDoc





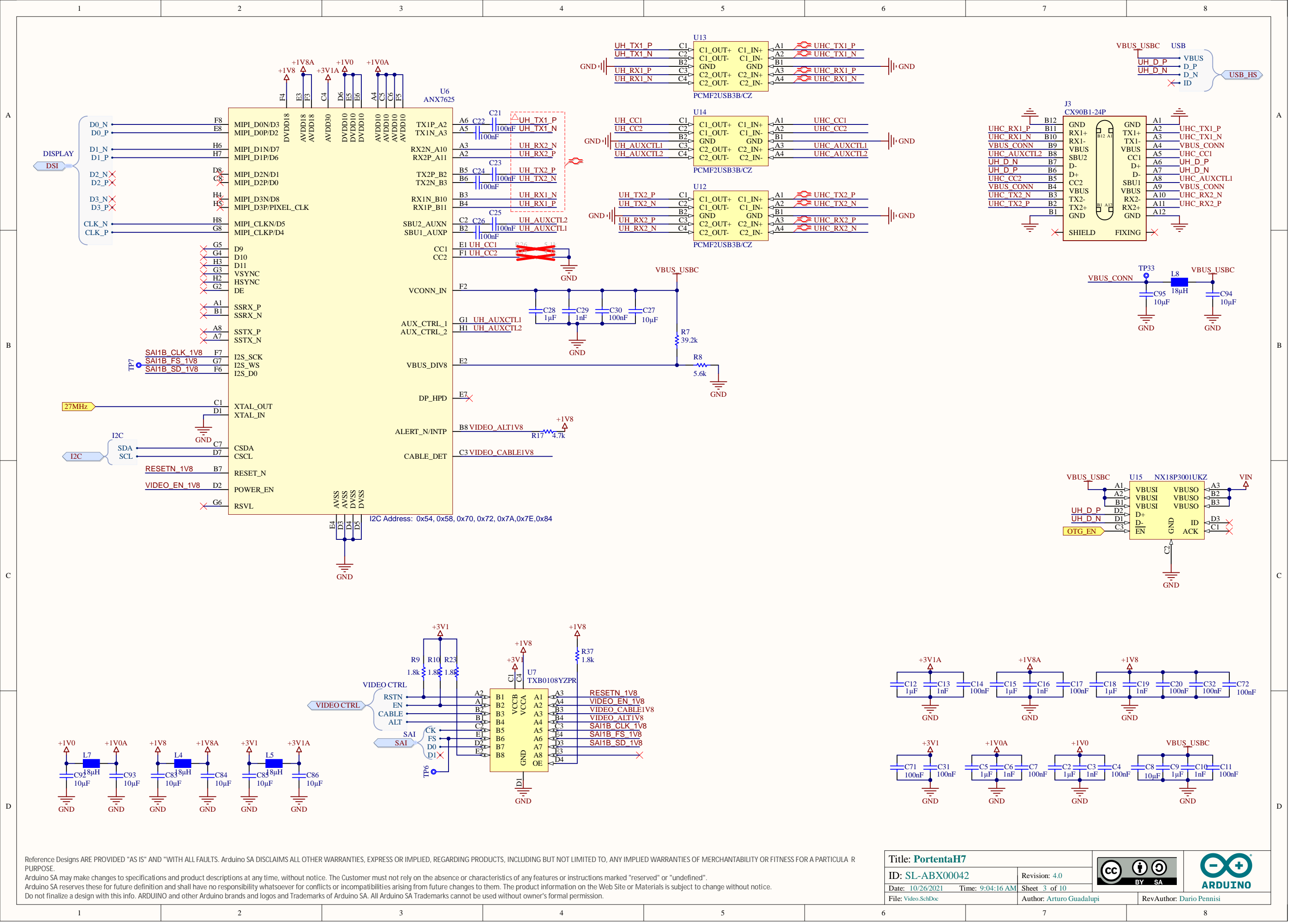
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Title: PortentaH7				
ID: SL-ABX00042		Revision: 4.0		
Date: 10/26/2021	Time: 9:04:11 AM	Sheet 1 of 10		
File: TopView.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi	



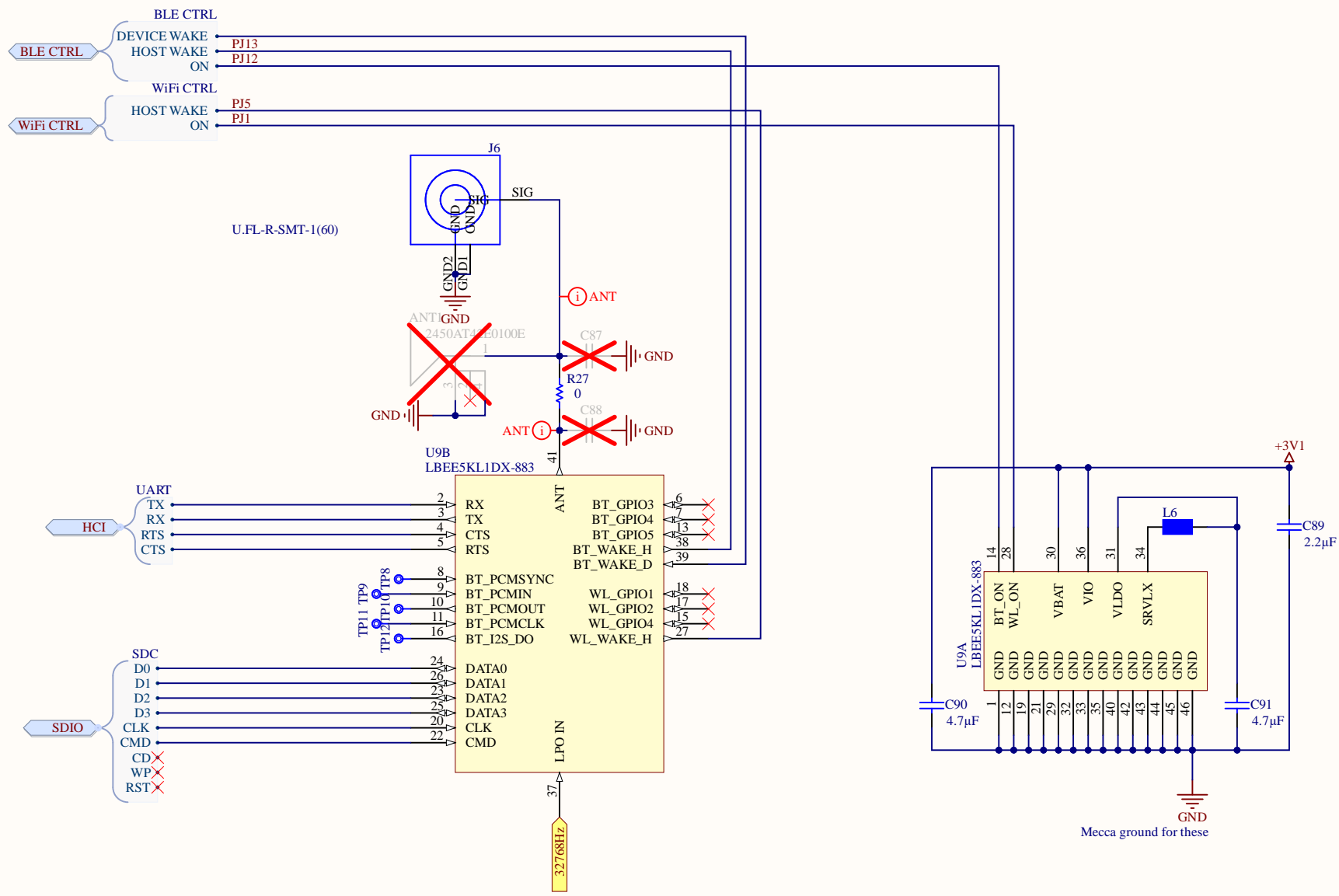
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Title: PortentaH7		 	
ID: SL-ABX00042			
Date: 10/26/2021	Time: 9:04:14 AM	Revision: 4.0	Sheet 2 of 10
File: STM32H747.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi



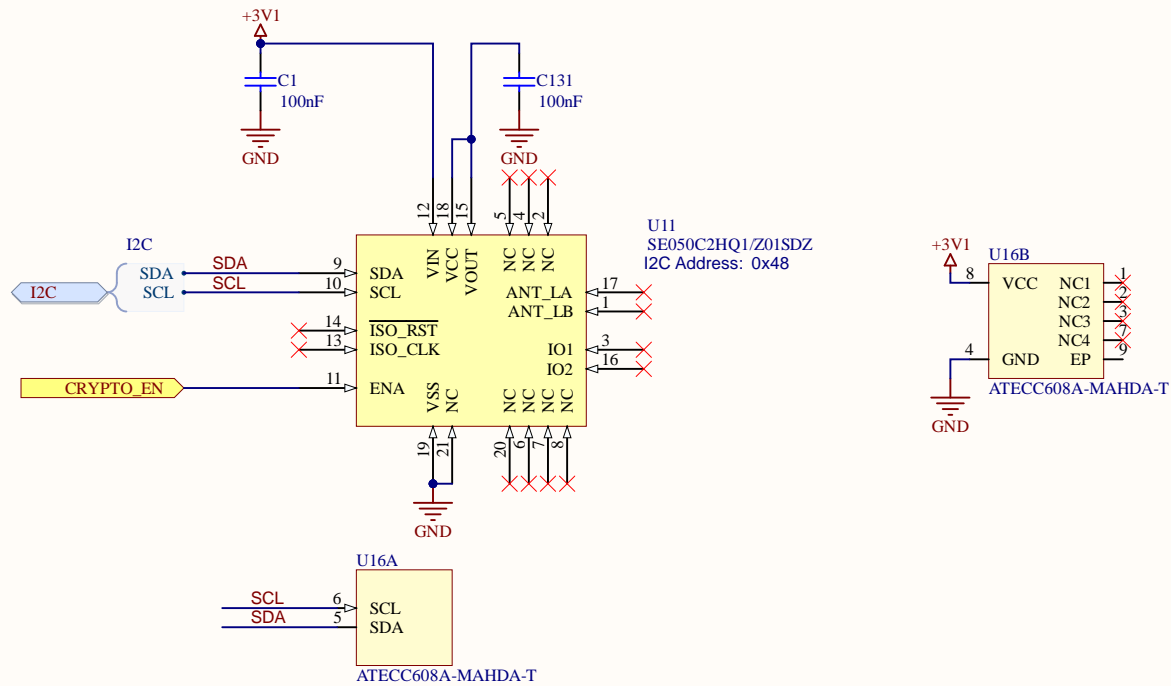
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Title: PortentaH7			
ID: SL-ABX00042	Revision: 4.0		
Date: 10/26/2021	Time: 9:04:16 AM	Sheet 3 of 10	
File: Video.SchDoc	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi	





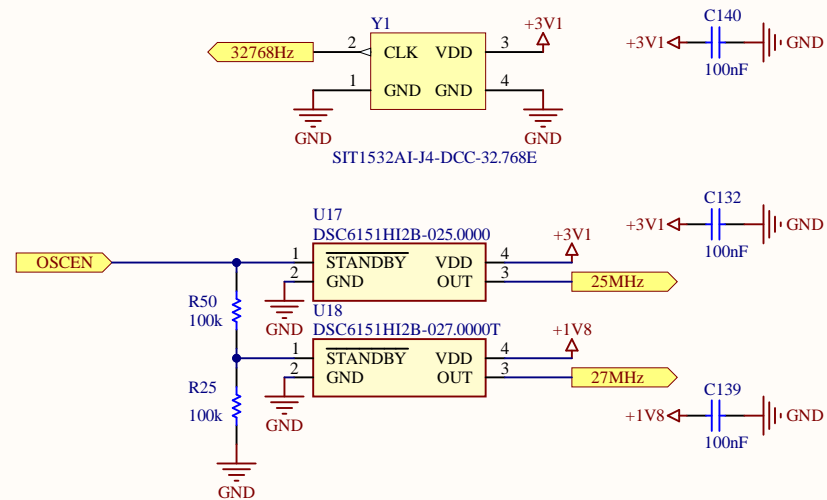
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Title: PortentaH7					
ID: SL-ABX00042		Revision: 4.0			
Date: 10/26/2021 Time: 9:04:20 AM		Sheet 4 of 10			
File: LBEE5KL1DX.SchDoc		Author: Arturo Guadalupi		RevAuthor: Dario Pennisi	





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Title: PortentaH7		 	
ID: SL-ABX00042	Revision: 4.0		
Date: 10/26/2021	Time: 9:04:23 AM	Sheet 5 of 10	
File: Cryptochip.SchDoc		Author: ArturoGuadalupi	RevAuthor: Dario Pennisi



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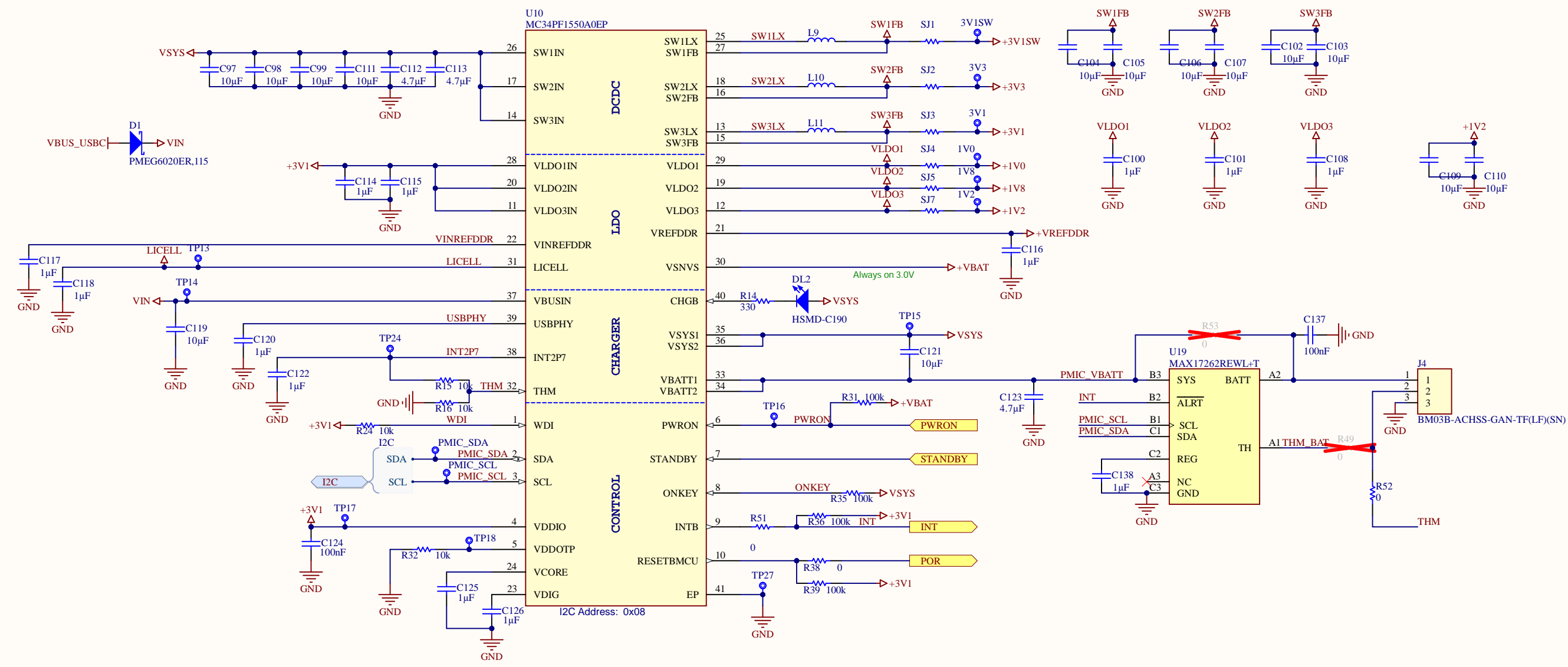
Title: PortentaH7		 	
ID: SL-ABX00042	Revision: 4.0		
Date: 10/26/2021	Time: 9:04:25 AM	Sheet 6 of 10	
File: Oscillators.SchDoc	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi	

A



B

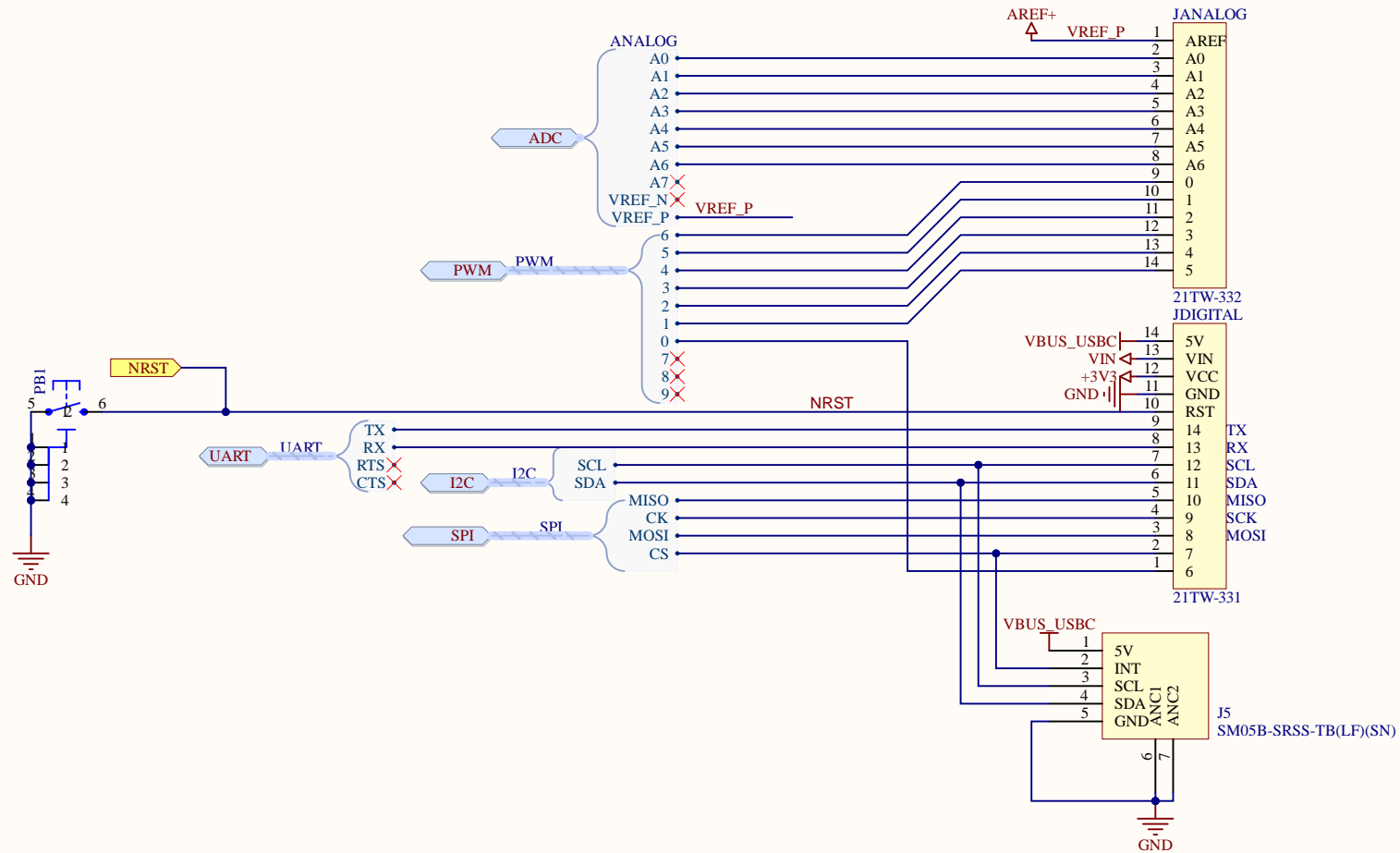
C

D





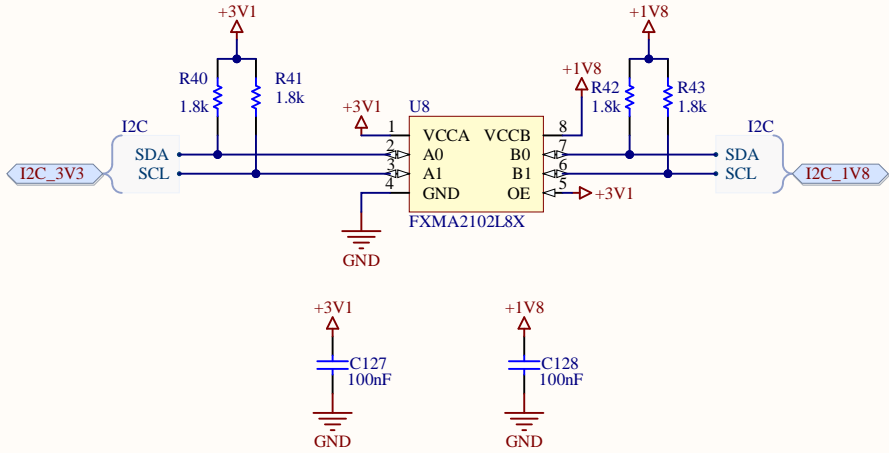
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Title: PortentaH7		 	
ID: SL-ABX00042	Revision: 4.0		
Date: 10/26/2021	Time: 9:04:27 AM	Sheet 7 of 10	
File: Power.SchDoc	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi	





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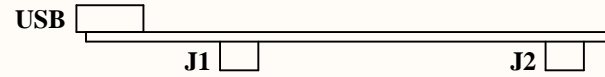
Title: PortentaH7		 	
ID: SL-ABX00042			
Date: 10/26/2021	Time: 9:04:30 AM	Sheet 8 of 10	
File: MKR.SchDoc		Author: Arturo Guadalupi	
		RevAuthor: Dario Pennisi	



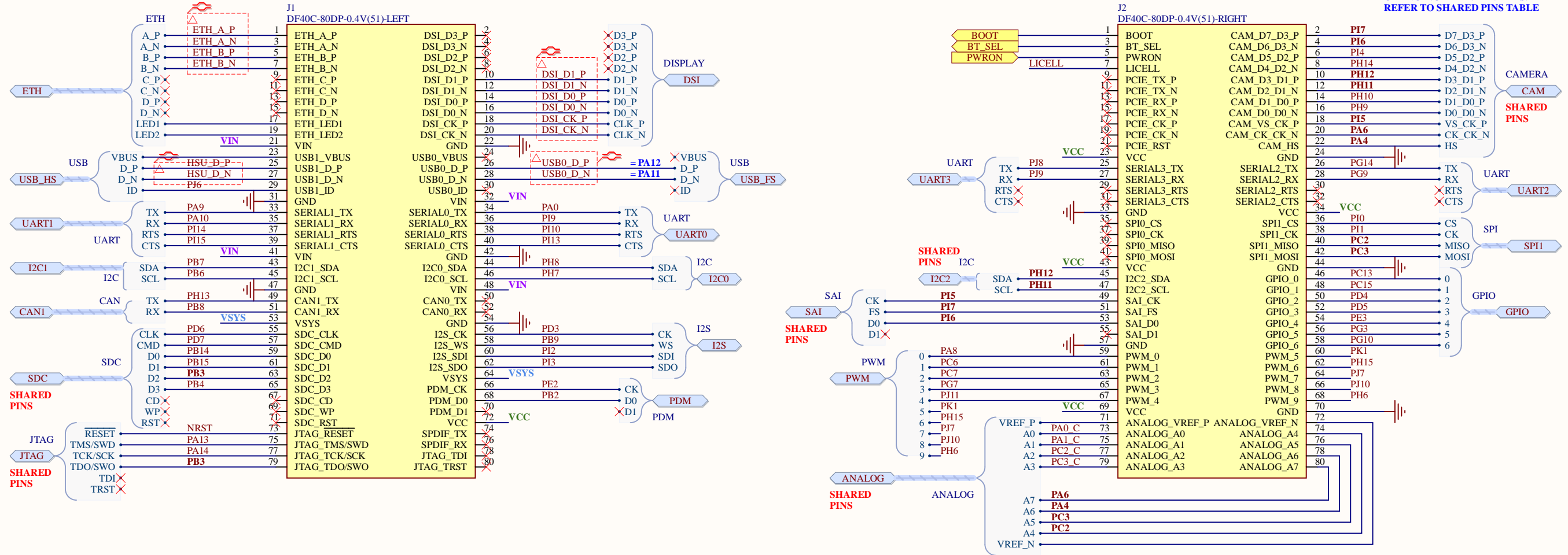
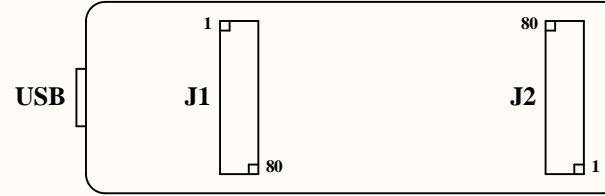
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Title: PortentaH7		 	
ID: SL-ABX00042			
Date: 10/26/2021 Time: 9:04:32 AM		Sheet 9 of 10	
File: I2CLevelShifter.SchDoc		Author: Arturo Guadalupi	
		RevAuthor: Dario Pennisi	

Board side view:



Board BOTTOM view:



IF NECESSARY ROUTE CAMERA WITH DIFFERENTIAL PAIR RULES CHANGING THE NET NAMES. REFER TO SHARED PINS TABLE

SHARED PINS TABLE

NET	BUS 1	BUS 2
PB3	JTAG	SDC2
PH11	CAM	I2C4
PH12	CAM	I2C4
PI5	CAM	SAI2A
PI6	CAM	SAI2A
PI7	CAM	SAI2A
PA4	CAM	ANALOG
PA6	CAM	ANALOG
PC2	ANALOG	SPI2
PC3	ANALOG	SPI2

POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U10) programmable output.
VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U10) programmable output.
VSYS	PORTENTA RESERVED OUTPUT	RESERVED, DO NOT USE 3.5V to 4.2V, max 600mA.	Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the bucks inside the PMIC itself.
LICELL	PORTENTA INPUT	Coinc cell max 3.6V, max 46uA.	Max 4uA with PMIC (U10) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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